PATENT ABSTRACTS OF JAPAN

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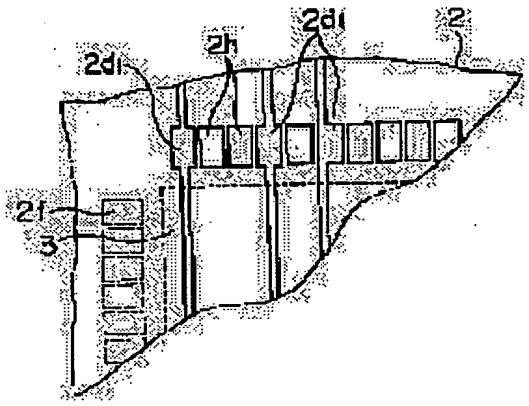
(54) THIN-FILM MULTI LAYER PRINTED CIRCUIT BOARD

(57)Abstract:

PURPOSE: To provide a thin-film multilayer printed circuit board suitable for forming a reliable multi-chip module easily, by eliminating a step part on faces of bonding pads formed in a row, and providing good conditions for bonding.

CONSTITUTION: On a main face of an insulating base board, a conductive wiring layer and an insulating layer are laminated alternately in a body, and a thin-film multilayer wiring part 2 made up of bonding pads in a row is formed at a given part of the upper face thereof. A conductive wiring in a layer provided just under a bonding pad (2f) of the thin-film multi layer wiring part 2 is so selected or set that the wiring width thereof becomes not less than that of the bonding pad (2f). Moreover, a dummy layer (2h) is formed in the other region under the bonding pad (2f) when there is no conductive wiring so that the face of the bonding pads in a row can be made flat.



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CLAIMS

[Claim(s)]
[Claim 1] In the thin film multilayer-interconnection substrate which possesses the thin film multilayer-interconnection section which carries out the laminating of a wiring layer and the electric insulation layer by turns and, by which the bonding pad has been made and arranged in the predetermined part on top seriate, and changes the conductor formed and arranged in one on a support substrate principal plane — the conductor by which the inner layer is carried out to the bonding pad directly under field of said thin film multilayer-interconnection section, while choosing and setting up wiring width of face at the width of face of a bonding pad, and the width of face of the same more than a conductor — the thin film multilayer-interconnection substrate characterized by having carried out the arrangement law of the dummy layer to other bonding pad directly under fields to which the inner layer of the wiring is not carried out, and carrying out flattening of said seriate bonding pad side.

[Translation done.] * NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a thin film multilayer-interconnection substrate, and relates to the thin film multilayer-interconnection substrate suitable for the configuration of a multi chip module or a hybrid IC in more detail.
[0002]
[Description of the Prior Art] In recent years, carrying and mounting the semiconductor device which miniaturization of electronic parts or an electronic circuitry, densification (large-capacity-izing), etc. are attained, for example, was package-ized at the so-called printed circuit board is known widely. however, the thin film multilayer-interconnection substrate which can be manufactured by the thin film technology with said conventional mounting means since there is a limitation in the densification (large-capacity-izing) etc. — the wiring substrate for mounting — carrying out — for example, — Development of the

multi chip module which carried and mounted the TAB (Tape Automated Bonding) chip is furthered. Drawing 3 is what showed the important section of the example of a configuration of such a thin film multilayer-interconnection substrate in cross section, on the predetermined field side of the insulating support substrate 1, has formed and arranged the so-called thin film multilayer-interconnection section 2 in one, and has accomplished the configuration which formed bonding pad 2f for connecting with electrode terminal 3a of the chip type element 3 carried and mounted electrically by the bonding wire 4 seriate on the maximum top face of the thin film multilayer-interconnection section 2. That is, they are power-source (conductor) layer 2a and thickness on the 1st page of an insulating support substrate. The insulating layer of the minerals system of about 100-150nm, For example SiO2 Layer 2b and grand (conductor) layer 2c further SiO2 layer 2b1, 2b2, 2b3, and a conductor (signal) — wiring layer 2d1, 2d2, and 2d3 A laminating and unification are carried out by turns. Bonding pad 2f which connects electrically to the maximum top face between die pad 2e which mounts a chip type element 3, and electrode terminal 3a of a chip type element 3 has accomplished the configuration arranged in one seriate corresponding to electrode terminal 3a of said chip type element 3. By the way, it sets in the thin film multilayer-interconnection section 2 of this seed thin film multilayer-interconnection plate, and is [as opposed to / generally / bonding pad 2f] 1, 2d2, and 2d3 2d of signal wiring layers. Wiring width of face is set up small (thinly). signal wiring layer 2d2 from which drawing 4 and drawing 5 differ, and 2d3 ******** — it is what showed typically patterning to bonding pad 2f on the top face of the maximum, and, in any case, wiring width of face is set as about 1 law.

[0003] In addition, in the above-mentioned configuration, 2d of signal wiring layers of the thin film multilayer-interconnection section 2, by 2g for example, of beer connection, it connects electrically and between 1, 2d2, 2d3, and bonding pad 2f forms the necessary wiring circuit.

[0004]

[Problem(s) to be Solved by the Invention] However, in the case of the thin film multilayer-interconnection substrate of said configuration, the following inconvenient problems are accepted. For example, the necessary chip type element 3 is mounted on the top face of the multilayer-interconnection section 2, and when carrying out wirebonding, the problem that bonding nature is inferior is in electrode terminal 3a of the chip type element 3, and corresponding bonding pad 2f. That is, it sets in the thin film multilayer-interconnection section 2, and, generally is 1, 2d2, and 2d3 2d of signal wiring layers. Since wiring width of face is small and narrower than the width of face which is bonding pad 2f, it is 1, 2d2, and 2d3 2d of this signal wiring layer. When bonding pad 2f is arranged on a wiring field, a level difference will arise inevitably. While this level difference generating of a bonding pad 2f page means irregularity-ization of a bonding pad 2f page and serves as difficulty [a bonding wire] of positioning, or the ease of happening of location gap, when it is based on a solder reflow etc., it will be accompanied by uneven soldering, and cannot attain mounting reliable as a result. If it explains in full detail to this point pan, it will set to this kind of thin film multilayer-interconnection plate. Layer insulation layer 2b1 of the thin film multilayer-interconnection section 2, 2b2, and 2b3 2-15 micrometers Extent and since it is thin, Signal wiring layer 2d1, 2d2, and 2d3 Existence or nonexistence etc. tend to affect the surface smoothness of thin film multilayer-interconnection section 2 front face. It is [as opposed to / as mentioned above / bonding pad 2f] 1, 2d2, and 2d3 2d of signal wiring layers with narrow width of face. Even if a inner layer and arrangement of are done, generating of a level difference is easily accepted in a directly under field. and such a phenomenon not only in each bonding pad 2f Between bonding pad 2f arranged seriate, Bonding pad with which inner layer and arrangement of 1, 2d2, and 2d3 are done 2d of signal wiring layers to directly under field if it puts in another way 2f, signal wiring layer 2d1, 2d2, and 2d3 A level difference arises also between a inner layer and bonding pad 2f which is not arranged. The surface smoothness as a bonding pad 2f train will be spoiled. Therefore, in said wirebonding etc., achievement of a homogeneity bonding operation of a bonding tool becomes difficult, and there is a problem that the dependability of bonding is easy to be spoiled.

[0005] This invention aims at offer of thin film multilayer-interconnection substrates which can be

constituted easily, such as a reliable multi chip module, by having coped with the above-mentioned situation, having been made, canceling the level difference of the bonding pad side arranged on the top face seriate, and giving good bonding nature.

[0006]

[Means for Solving the Problem] The laminating of a wiring layer and the electric insulation layer is carried out by turns. the conductor with which the thin film multilayer-interconnection substrate concerning this invention has been formed and arranged in one on a support substrate principal plane — And it sets to the thin film multilayer-interconnection substrate with which a bonding pad possesses in seriate the thin film multilayer-interconnection section made and arranged, and grows into a predetermined part on top. the conductor by which the inner layer is carried out to the bonding pad directly under field of said thin film multilayer-interconnection section, while choosing and setting up wiring width of face the same above as the width of face of a bonding pad a conductor — wiring is characterized by having carried out the arrangement law of the dummy layer to other bonding pad directly under fields by which a inner layer is not carried out, and carrying out flattening of said seriate bonding pad side.

[0007]

[Function] In the field which is located directly under the bonding pad currently arranged in the top face by seriate among the signal wiring of the multilayer-interconnection section according to this invention Huge-ize the signal wiring width of face superficially, and while the bonding pad located in said upper layer takes the configuration which can hold a flat surface, in the directly under field of other bonding pads with which signal wiring does not exist in directly under, the inner layer and arrangement of a dummy layer are done. It is formed so that a bonding pad train may take surface smoothness on the whole. That is, since level difference attachment of the seriate bonding pad side resulting from the inner layer of signal wiring is avoided easily and certainly (dissolution) and is presenting flat-surface (flat) nature good on the whole, it is improved and improved sharply, and the reliable bonding of bonding nature becomes possible, and it contributes to the configuration of the multi chip module which was excellent in quality greatly.

[0008]

[Example] Hereafter, one example of this invention is explained with reference to drawing 1 – drawing 3 .

[0009] The thin film multilayer-interconnection substrate concerning this invention can be said to be the same as that of the conventional case in the fundamental configuration. That is, as the example of an important section configuration was shown in said drawing 3 in cross section, the configuration has formed and arranged the so-called thin film multilayer-interconnection section 2 in one on the predetermined field side of the support substrate 1, and has accomplished the configuration in which bonding pad 2f for [which is carried and mounted] connecting electrically electrode terminal 3a of a chip type element 3, for example was formed, in the maximum top face of the thin film multilayer-interconnection section 2. When it furthermore explains in full detail, they are power-source (conductor) layer 2a and thickness on the 1st page of a support substrate. The insulating layer of the minerals system of about 100-150nm, For example SiO2 Layer 2b and grand (conductor) layer 2c further SiO2 layer 2b1, 2b2, 2b3, and a conductor (signal) — wiring layer 2d1, 2d2, and 2d3 A laminating and unification are carried out by turns. The configuration that bonding pad 2f which connects electrically to the maximum top face die pad 2e which mounts a chip type element 3, and electrode terminal 3a of a chip type element 3 by wirebonding 4 has been arranged in one seriate is accomplished.

[0010] By the way, it sets to the thin film multilayer-interconnection plate concerning this invention, and characterizes in that a part of configuration of said thin film multilayer-interconnection section 2 was changed and set up as follows. Namely, signal wiring layer 2d1 located in the directly under field of it to bonding pad 2f prepared in seriate [said], 2d2, and 2d3 While setting wiring width of face as the configuration huge-ized especially alternatively Signal wiring is doing the inner layer and arrangement of the same area as a bonding pad 2f page, or 2h (layer) of a little larger dummy pieces in the field which

does not exist in directly under. the signal wiring layer from which drawing 1 and drawing 2 differ mutually, signal wiring layer 2d2 [for example,], and 2d3 It is what showed typically patterning to bonding pad 2f on the top face of the maximum. ******** — In any case, the signal wiring width of face located in a bonding pad 2f field [directly under] While setting up enormously a little more greatly alternatively, in the same width of face as said bonding pad 2f piece thru/or the field to which signal wiring does not exist, the inner layer and arrangement of the same area as a bonding pad 2f page thru/or 2h (layer) of a little larger dummy pieces are done. In addition, it sets in the above-mentioned configuration and is 1, 2d2, and 2d3 2d of signal wiring layers of the thin film multilayer-interconnection section 2. And by 2g for example, of beer connection, it connects electrically and between bonding pad 2f forms the necessary wiring circuit.

[0011] The thin film multilayer-interconnection plate concerning above-mentioned this invention can be easily manufactured based on the manufacture means usually taken in manufacture of this seed thin film multilayer-interconnection plate. That is, they are said insulating-layer 2b1, 2b2, and 2b3 with the obligatory manufacture means of this kind of thin film multilayer-interconnection plate. And signal wiring layer 2d1, 2d2, and 2d3 The part of an alternation and laminating chemically-modified degree is changed. Signal wiring layer 2d1, 2d2, and 2d3 In a patterning process While setting up alternatively enormously a part of signal wiring arranged directly under the bonding pad 2f train planned on a design It can manufacture easily only by adding the actuation which inserts and arranges suitably 2h of dummy layers, such as a piece of a metal, a resin layer, etc. from which said signal wiring and comparable thickness were insulated, in a predetermined location (field) to the other bonding pad 2f directly under field similarly planned on a design.

[0012] This invention is not limited to the above-mentioned instantiation, and can take deformation various in the range which does not deviate from the main point of invention. That is, as a support substrate, it is not restricted to a silicon substrate with an oxide film, for example, is aluminum 2O3. A substrate, a polyimide resin system substrate, Si substrate formed into low resistance, etc. may be used, and it is also the insulating layer of the multilayer-interconnection section. SiO2 Instead of a layer, for example, a glass layer, a polyimide resin layer, a benz-cyclo-butene resin layer, etc. are sufficient. Moreover, the quality of the materials, such as a voltage plane, a grand layer, and a signal wiring layer, are also chosen suitably.

[0013]

[Effect of the Invention] In the thin film multilayer-interconnection substrate applied to this invention as explained above In the directly under field of the seriate bonding pad currently arranged in the top face among the signal wiring of the multilayer-interconnection section Huge-ize the signal wiring width of face superficially, and while the bonding pad located in said upper layer takes the configuration which can hold a flat surface, in the field to which signal wiring does not exist directly under other bonding pads, the inner layer and arrangement of a dummy layer are done. It is formed so that the bonding pad side which accomplishes seriate may take uniform surface smoothness. That is, since level difference attachment of the bonding pad side resulting from signal wiring is avoided easily on the whole and certainly (dissolution) and is presenting good flat-surface (flat) nature, it is improved and improved sharply, and the reliable bonding of bonding nature becomes possible, and it contributes to the configuration of the multi chip module which was excellent in quality greatly.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The top view showing the important section of the example of patterning of the 1 signal wiring layer of the thin film multilayer-interconnection substrate concerning this invention.
[Drawing 2] The top view showing the important section of the example of patterning of other signal wiring layers of the thin film multilayer-interconnection substrate concerning this invention.
[Drawing 3] The sectional view showing the important section configuration of a thin film multilayer-interconnection substrate.
[Drawing 4] The top view showing the important section of the example of patterning of the 1 signal wiring layer of the conventional thin film multilayer-interconnection substrate.
[Drawing 5] The top view showing the important section of the example of patterning of other signal wiring layers of the conventional thin film multilayer-interconnection substrate.
[Description of Notations]
1 — support substrate 2 — thin film multilayer-interconnection section 2a— voltage plane 2b— insulating layer 2c and 5c— grand layer 2b1, 2b2, and 2b3 — layer insulation layer 2d1, 2d2, and 2d3 — signal wiring layer 2e— die pad 2f— bonding pad 2g— beer connection 2h — Dummy layer (piece) 3 — Chip type element 3a — Electrode terminal of a chip type element
4 — Bonding wire

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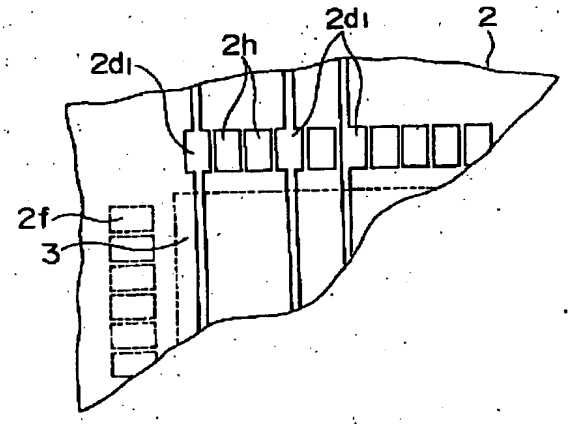
(54)【発明の名称】　薄膜多層配線基板

(57)【要約】
【目的】　上面に列状に配置されているボンディングパッド面の段差を解消し、良好なボンディング性を持たせることにより、信頼性の高いマルチチップモジュールなど容易に構成し得る薄膜多層配線基板の提供を目的とする。
【構成】　絶縁性支持基板主面上に一体的に形成・配置された導体配線層および電気絶縁層を交互に積層し、かつ上面の所定箇所にボンディングパッドが列状に形設・配置された薄膜多層配線部とを具備して成る薄膜多層配線基板において、前記薄膜多層配線部２のボンディングパッド2f直下領域に内層されている導体配線幅をボンディングパッド2fの幅と同一以上に選択・設定するとともに、導体配線が内層されていない他のボンディングパッド2f直下領域にダミー層2hを配設定して、前記列状のボンディングパッド2f面を平坦化させたことを特徴とする。



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【特許請求の範囲】

【請求項１】 支持基板主面上に一体的に形成・配置された導体配線層および電気絶縁層を交互に積層し、かつ上面の所定箇所にボンディングパッドが列状に形設・配置された薄膜多層配線部を具備して成る薄膜多層配線基板において、

前記薄膜多層配線部のボンディングパッド直下領域に内層されている導体配線幅をボンディングパッドの幅と同一以上の幅に選択・設定するとともに、導体配線が内層されていない他のボンディングパッド直下領域にダミー層を配設定して、前記列状のボンディングパッド面を平坦化させたことを特徴とする薄膜多層配線基板。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は薄膜多層配線基板に係り、さらに詳しくは、マルチチップモジュールやハイブリッドICの構成に適する薄膜多層配線基板に関する。

【０００２】

【従来の技術】近年、電子部品もしくは電子回路の小形化，高密度化（大容量化）などが図られており、たとえばパッケージ化した半導体装置を、いわゆるプリント基板に搭載・実装することが広く知られている。しかし、前記従来の実装手段では、その高密度化（大容量化）などに限界があるため、薄膜技術によって製造し得る薄膜多層配線基板を実装用の配線基板とし、たとえばTAB(Tape Automated Bonding)チップを搭載・実装したマルチチップモジュールなどの開発が進められている。図３はこのような薄膜多層配線基板の構成例の要部を断面的に示したもので、絶縁性支持基板１の所定領域面上に、いわゆる薄膜多層配線部２を一体的に形成・配置し、その薄膜多層配線部２の最上面には搭載・実装するチップ素子３の電極端子3aにボンディングワイヤ４により電気的に接続するためのボンディングパッド2fを列状に形成した構成を成している。すなわち、絶縁性支持基板１面上に、電源（導体）層2a，厚さ 100～ 150nm程度の無機質系の絶縁層，たとえば SiO_2 層2b，グランド（導体）層2cを、さらに、SiO_2 層$2b_1$，$2b_2$，$2b_3$、導体（信号）配線層$2d_1$，$2d_2$，$2d_3$ を交互に積層・一体化し、最上面にはチップ素子３をマウントするダイパッド2e、およびチップ素子３の電極端子3aとの間を電気的に接続するボンディングパッド2fが、前記チップ素子３の電極端子3aに対応して列状に一体的に配置された構成を成している。 ところで、この種薄膜多層配線板の薄膜多層配線部２においては、一般的にボンディングパッド2fに対して、信号配線層$2d_1$，$2d_2$，$2d_3$ の配線幅が小さく（細く）設定されている。図４および図５は、異なる信号配線層$2d_2$，$2d_3$ について、最上面のボンディングパッド2fに対するパターニングを模式的に示したもので、いずれの場合も配線幅がほぼ一定に設定されている。

【０００３】なお、上記構成においては、薄膜多層配線

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部２の信号配線層$2d_1$，$2d_2$，$2d_3$およびボンディングパッド2f間が、たとえばビア接続2gによって電気的に接続され、所要の配線回路を形成している。

【０００４】

【発明が解決しようとする課題】しかし、前記構成の薄膜多層配線基板の場合は、次のような不都合な問題が認められる。たとえば、多層配線部２の上面に所要のチップ素子３をマウントし、そのチップ素子３の電極端子3aと対応するボンディングパッド2fに、ワイヤボンディングする場合など、ボンディング性が劣るという問題がある。つまり、薄膜多層配線部２においては、一般的に信号配線層$2d_1$，$2d_2$，$2d_3$ の配線幅が小さく、ボンディングパッド2fの幅よりも狭いため、この信号配線層$2d_1$，$2d_2$，$2d_3$ の配線領域上にボンディングパッド2fが配置されると必然的に段差が生じることになる。このボンディングパッド2f面の段差発生は、ボンディングパッド2f面の凹凸化を意味し、ボンディングワイヤの位置決めの困難さ、もしくは位置ズレの起こり易さとなる一方、また半田リフローなどによる場合は不均一な半田付けを伴うことになり、結果的に信頼性の高い実装を達成し得ないことになる。この点さらに詳述すると、この種の薄膜多層配線板においては、薄膜多層配線部２の層間絶縁層$2b_1$，$2b_2$，$2b_3$ が 2～15μm 程度と薄いため、信号配線層$2d_1$，$2d_2$，$2d_3$ の存否なども薄膜多層配線部２表面の平坦性に影響を及ぼし易く、前記のようにボンディングパッド2fに対して幅の狭い信号配線層$2d_1$，$2d_2$，$2d_3$ が直下領域に内層・配置されていても、段差の発生が容易に認められる。そして、このような現象は個々のボンディングパッド2fだけでなく、列状に配置されているボンディングパッド2f間、換言すると直下領域に信号配線層$2d_1$，$2d_2$，$2d_3$が内層・配置されているボンディングパッド2fと信号配線層$2d_1$，$2d_2$，$2d_3$ が内層・配置されていないボンディングパッド2fとの間でも段差が生じ、ボンディングパッド2f列としての平坦性が損なわれることになる。したがって、前記ワイヤボンディングなどにおいて、たとえばボンディングツールの均一的なボンディング作用の達成が困難となり、ボンディングの信頼性が損なわれ易いという問題がある。

【０００５】本発明は上記事情に対処してなされたもので、上面に列状に配置されているボンディングパッド面の段差を解消し、良好なボンディング性を持たせることにより、信頼性の高いマルチチップモジュールなど容易に構成し得る薄膜多層配線基板の提供を目的とする。

【０００６】

【課題を解決するための手段】本発明に係る薄膜多層配線基板は、支持基板主面上に一体的に形成・配置された導体配線層および電気絶縁層を交互に積層し、かつ上面の所定箇所にボンディングパッドが列状に形設・配置された薄膜多層配線部を具備して成る薄膜多層配線基板において、前記薄膜多層配線部のボンディングパッド直下

領域に内層されている導体配線幅をボンディングパッドの幅と同一以上に選択・設定するとともに、導体配線が内層されていない他のボンディングパッド直下領域にダミー層を配設定して、前記列状のボンディングパッド面を平坦化させたことを特徴とする。

【０００７】

【作用】本発明によれば、多層配線部の信号配線のうち、上面に列状に配設されているボンディングパッドの直下に位置する領域において、その信号配線幅を平面的に膨大化して、前記上層に位置するボンディングパッドが平面を保持し得る構成を採る一方、信号配線が直下に存在しない他のボンディングパッドの直下領域にはダミー層を内層・配置して、ボンディングパッド列が全体的に平坦性を採るよう形成されている。つまり、信号配線の内層に起因する列状のボンディングパッド面の段差付けが容易、かつ確実に回避（解消）されて、全体的に良好な平面（平坦）性を呈しているため、ボンディング性が大幅に向上・改善され、信頼性の高いボンディングが可能となり、品質のすぐれたマルチチップモジュールなどの構成に大きく寄与する。

【０００８】

【実施例】以下、図１～図３を参照して本発明の一実施例を説明する。

【０００９】本発明に係る薄膜多層配線基板は、その基本的な構成においては従来の場合と同様といえる。すなわち、その構成は、前記図３に要部構成例を断面的に示したごとく、支持基板１の所定領域面上に、いわゆる薄膜多層配線部２を一体的に形成・配置し、その薄膜多層配線部２の最上面には搭載・実装するたとえばチップ素子３の電極端子3aを電気的に接続するためのボンディングパッド2fを形成した構成を成している。さらに詳述すると、支持基板１面上に、電源（導体）層2a，厚さ 100～150nm程度の無機質系の絶縁層、たとえば SiO_2 層2b，グランド（導体）層2cを、さらに、SiO_2 層$2b_1$，$2b_2$，$2b_3$、導体（信号）配線層$2d_1$，$2d_2$，$2d_3$ を交互に積層・一体化し、最上面にはチップ素子３をマウントするダイパッド2e、およびチップ素子３の電極端子3aをワイヤボンディング４により電気的に接続するボンディングパッド2fが列状に一体的に配置された構成を成している。

【００１０】ところで、本発明に係る薄膜多層配線板においては、前記薄膜多層配線部２の構成の一部を、次のように変更・設定した点で特徴付けられる。すなわち、前記列状に設けられているボンディングパッド2fに対して、その直下領域に位置する信号配線層$2d_1$，$2d_2$，$2d_3$ の配線幅を、特に、選択的に膨大化した形状に設定するとともに、信号配線が直下に存在しない領域にはボンディングパッド2f面と同一面積もしくはやや大きめのダミー片（層）2hを内層・配置している。図１および図２は、互いに異なる信号配線層、たとえば信号配線層2

d_2，$2d_3$ について、最上面のボンディングパッド2fに対するパターニングを模式的に示したもので、いずれの場合も、ボンディングパッド2fの直下の領域に位置する信号配線幅を、前記ボンディングパッド2f幅と同一幅ないしやや大きめに選択的に膨大に設定する一方、信号配線が存在しない領域にはボンディングパッド2f面と同一面積ないしやや大きめのダミー片（層）2hが内層・配置されている。なお、上記構成においては、薄膜多層配線部２の信号配線層$2d_1$，$2d_2$，$2d_3$ およびボンディングパッド2f間が、たとえばビア接続2gによって電気的に接続され、所要の配線回路を形成している。

【００１１】上記本発明に係る薄膜多層配線板は、この種薄膜多層配線板の製造において通常採られている製造手段に基づいて容易に製造し得る。すなわち、この種の薄膜多層配線板の常套的な製造手段で、前記絶縁層2b_1，$2b_2$，$2b_3$ および信号配線層$2d_1$，$2d_2$，$2d_3$ の交互・積層化工程の一部を変更し、信号配線層$2d_1$，2d2，$2d_3$ のパターニング工程において、設計上予定しているボンディングパッド2f列の直下に配設される信号配線の一部を選択的に膨大に設定する一方、同じく設計上予定している他のボンディングパッド2fの直下領域には、前記信号配線と同程度厚の絶縁された金属片や樹脂層などダミー層2hを所定位置（領域）に、適宜介挿・配設する操作を加えるだけで容易に製造し得る。

【００１２】本発明は上記例示に限定されるものでなく、発明の主旨を逸脱しない範囲で種々の変形を採り得る。すなわち、支持基板としては、酸化膜付きのシリコン基板に限られず、たとえばAl_2O_3 基板やポリイミド樹脂系基板、低抵抗化したSi基板などでもよいし、多層配線部の絶縁層も SiO_2 層の代わりに、たとえばガラス層、ポリイミド樹脂層やベンゾシクロブテン樹脂層などでもよい。また、電源層，グランド層，信号配線層などの材質も適宜選択される。

【００１３】

【発明の効果】以上説明したように、本発明に係る薄膜多層配線基板においては、多層配線部の信号配線のうち、上面に配設されている列状のボンディングパッドの直下領域では、その信号配線幅を平面的に膨大化して、前記上層に位置するボンディングパッドが平面を保持し得る構成を採る一方、他のボンディングパッドの直下に信号配線が存在しない領域にはダミー層を内層・配置して、列状を成すボンディングパッド面が一様の平坦性を採るように形成されている。つまり、信号配線に起因するボンディングパッド面の段差付けが全体的に容易、かつ確実に回避（解消）されて、良好な平面（平坦）性を呈しているため、ボンディング性が大幅に向上・改善され、信頼性の高いボンディングが可能となり、品質のすぐれたマルチチップモジュールなどの構成に大きく寄与する。

【図面の簡単な説明】

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【図１】本発明に係る薄膜多層配線基板の一信号配線層のパターニング例の要部を示す平面図。

【図２】本発明に係る薄膜多層配線基板の他の信号配線層のパターニング例の要部を示す平面図。

【図３】薄膜多層配線基板の要部構成を示す断面図。

【図４】従来の薄膜多層配線基板の一信号配線層のパターニング例の要部を示す平面図。

【図５】従来の薄膜多層配線基板の他の信号配線層のパターニング例の要部を示す平面図。

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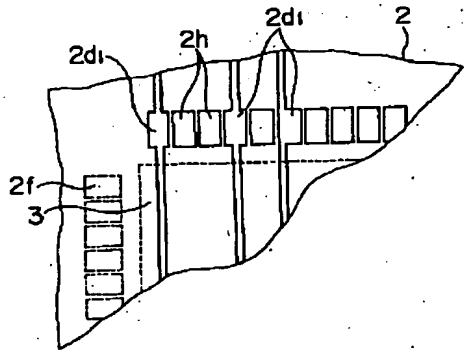
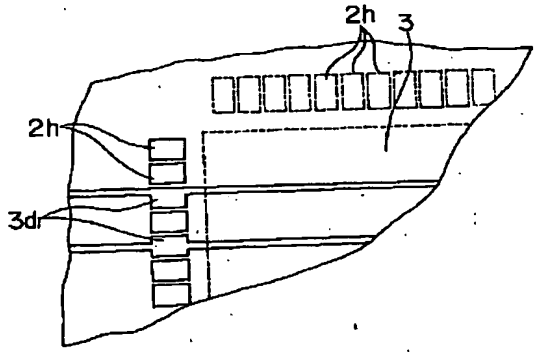
【符号の説明】

1…支持基板　2…薄膜多層配線部　2a…電源層　2b…絶縁層　2c，5c…グランド層　$2b_1$，$2b_2$，$2b_3$…層間絶縁層　$2d_1$，$2d_2$，$2d_3$…信号配線層　2e…ダイパッド　2f…ボンディングパッド　2g…ビア接続　2h…ダミー層（片）　3…チップ素子　3a…チップ素子の電極端子　4…ボンディングワイヤ

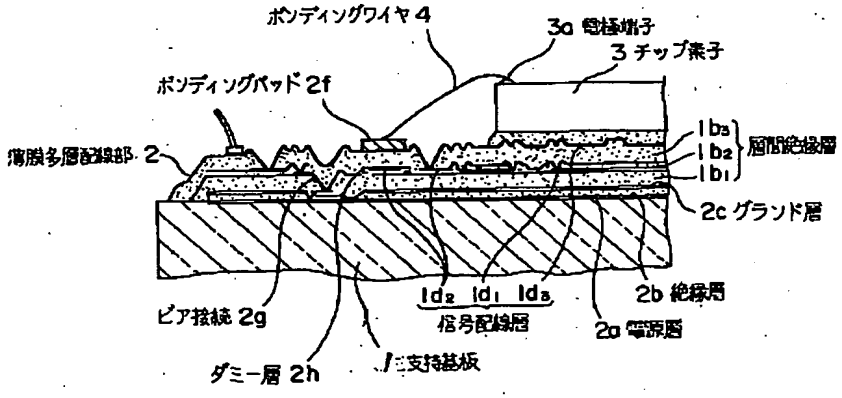
【図１】



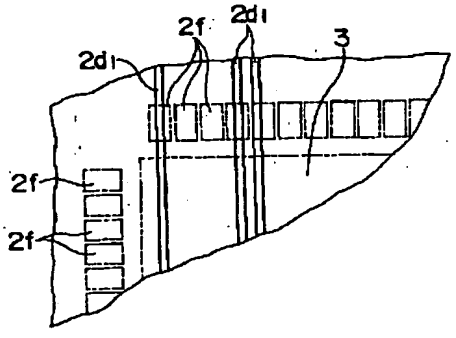
【図２】



【図３】



【図４】



【図５】